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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,906	08/26/2003	William Robert Haas	100201032-1	5761

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
GOLDEN, JAMES R	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,906	HAAS ET AL.	
	Examiner	Art Unit	
	James Golden	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This action is in response to the communication received December 15, 2005 with the amendments to claims 1, 3, 8 and 12, and the cancellation of claims 10-11. Claims 1-9 and 12 are currently pending in the application.

Drawings

1. The corrections to the references to drawings received on December 15, 2005 are accepted by the examiner, and the objections are withdrawn.

Specification

2. The corrections to the specification received on December 15, 2005 are accepted by the examiner, and the objections are withdrawn.

Claim Objections

3. The corrections to claims 3 and 8 received on December 15, 2005 are accepted by the examiner, and the objections to claims 3-9 are withdrawn.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1 and 3-5** are rejected under 35 U.S.C. 102(b) as being anticipated by Krech, Jr. et al. (US 5,664,114).

6. **With respect to claim 1**, Krech, Jr. et al. disclose a memory control system, comprising:

- a processor (110 of Fig. 1);
- a bus in communication with the processor (input line to 102 of Fig. 1);
- a first memory (115 of Fig. 1) removed from said processor (interpreted as external to the processor) in communication with the processor in a first data path removed from the bus (connection from microprocessor to FIFO 115); and
- a second memory (112 of Fig. 1) removed from said processor (interpreted as external to the processor) in communication with the processor in a second data path removed from the bus (connection from microprocessor to FIFO 112) and
- having an empty memory indicator (column 5, lines 10-12);
- wherein, in response to the second memory containing no application data, the second memory provides a corresponding indication to the processor (column 5, lines 10-12).

7. **With respect to claim 3**, Krech, Jr. et al. disclose a memory control system, comprising:

- a controller module (110 of Fig. 1) having
    - a first data path ("memory" of 111 of Fig. 1 on board 110; column 4, line 11),
    - a second data path (connection from microprocessor 110 to memory 112), and

- a bus (input line to 102 of Fig. 1); and
- a first memory in communication with the first data path ("memory" of 111 of Fig. 1); and
- a second memory in communication with the second data path (112 of Fig. 1) and having
- an empty memory indicator (column 5, lines 10-12);

- wherein the controller module replicates data from the first memory to the second memory in response to an empty data indication from the second memory (column 6, lines 43-49).

8. **With respect to claim 4**, Krech, Jr. et al. disclose the system of claim 3, further comprising:

- an application module (102 of Fig.1) in communication with (connection from 102 to 105 and 105 to 110) the controller module (110 of Fig.1),
- wherein the controller module is connected to retrieve application data from the application module for storage in the first memory (column 3, line 67 – column 4, lines 1-2).

9. **With respect to claim 5**, Krech, Jr. et al. disclose the system of claim 3, further comprising:

- a memory module (composition of "memory" of 111 and 112 of Fig. 1) in communication with (111 on board 110, and connection from 110 to 112) the controller module (110 of Fig. 1) and
- containing the first memory ("memory" of 111 of Fig. 1) and the second memory (112 of Fig. 1).

10. **Claims 8-9** are rejected under 35 U.S.C. 102(b) as being anticipated by Baentsch et al. (US 6,272,607).

11. **With respect to claim 8**, Baentsch et al. disclose a method of installing a new memory (9 of Fig. 1) that has a predetermined memory capacity into a system that comprises a processor (1 of Fig. 1) and first old memory (51 of Fig. 1), with the first old memory storing an amount of application data to produce a redundant array of independent memories, comprising:

- initiating a duplication function in the processor (column 3, lines 9-15);
- transmitting an empty data indication from the new memory to the processor (column 2, lines 61-67 – column 3, lines 1-2); and
- replicating the application data from the first old memory to the new memory (column 3, lines 17-18 describe how the "data space" 5 of Fig. 1 of memory 9 of Fig. 1 is "filled with the object payload;" column 5, lines 57-58 describe how the payload data is "transmitted in segments from the RAM 51 to the EEPROM 50," where the EEPROM contains memory block 9).

12. **With respect to claim 9**, Baentsch et al. disclose the method of claim 8 (see above paragraph 11, wherein replicating the application data comprises comparing the amount of application data in the first old memory to the capacity of the new memory to determine whether said capacity is sufficient to hold the application data (column 3, lines 11-12).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. **Claims 2, 6 and 7** are rejected under 35 U.S.C. 103(a) as being unpatentable over Krech, Jr. et al. (5,664,114) as applied to claims 1 and 3-5 above (see paragraphs 6-9), in view of McNutt et al. (US 5,659,705).

15. **With respect to claim 2**, Krech, Jr. et al. disclose the system of claim 1 (see above paragraph 6). Krech, Jr. et al. do not disclose the limitations further comprising a hub in communication with the bus to provide application data to the processor.

However, McNutt et al. disclose the limitations further comprising a hub (26 of Fig. 1; column 6, lines 12-13, 20-26) in communication with the bus (32 of Fig. 1; column 6, lines 11-13) to provide application data to the processor (Fig. 5; column 4, lines 60-63).

Krech, Jr. et al. and McNutt et al. are analogous art because they are from the same field of endeavor, namely the transfer of data between memories.

At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the hub of McNutt et al. with the architecture of Krech, Jr. et al. The motivation for doing so would have been so that the system of Krech, Jr. et al. could "transport the user program and data to another PLC [programmable logic controller]" (column 4, line 63).

Therefore, it would have been obvious to combine McNutt et al. with Krech, Jr. et al. for the benefit of a system connected to a network to obtain the invention as specified in claim 2.

16. **With respect to claim 6**, Krech, Jr. et al. disclose the system of claim 3 (see above paragraph 7). Krech, Jr. et al. fail to disclose the limitations further comprising:

- an application electrical connector on the application module; and
- a controller electrical connector on the electrical applications controller in communication with the application electrical connector;
- wherein each of said electrical connectors are axially symmetric to enable different relative rotational positions between the application and connector modules.

However, McNutt et al. disclose

- an application electrical connector on the application module ("Bus Expansion Port" or 32 on "Expansion Module" of Fig. 1); and
- a controller electrical connector on the electrical applications controller in communication with the application electrical connector (32 of Fig. 1);
- wherein each of said electrical connectors are axially symmetric to enable different relative rotational positions between the application and connector modules (Fig. 5).

It should be noted that the axis of symmetry is not specified in the drawings. The examiner has assumed the axis "running through the application module 165" (Detailed Description, page 11, lines 302-303) to be a line drawn perpendicularly to the face of the application module with connector 415 at its center, shown in Fig. 4. The

connectors shown in Fig. 5 of McNutt et al. are clearly symmetric about an analogous axis, drawn perpendicularly to the face of 32 of Fig. 5 at its center.

Krech, Jr. et al. and McNutt et al. are analogous art because they are from the same field of endeavor, namely the transfer of data between memories.

At the time of invention it would have been obvious to a person of ordinary skill in the art to apply the portability of the device of McNutt et al. to the architecture of Krech, Jr. et al. McNutt et al. teach the motivation for doing so as "a memory cartridge which may be reprogrammed in place by user command, then used to transport the user program and data to another PLC [programmable logic controller]" (column 4, lines 61-63). Therefore, it would have been obvious to combine Krech, Jr. et al. with McNutt et al. for the benefit of a portable data-transfer and storage device as specified in claim 6.

17. **Claim 7** distinguishes over the teaching of Krech, Jr. et al. by the limitations of means for releasably connecting the application module to the electrical applications controller ("Bus Expansion Port" or 32 on "Expansion Module" of Fig. 1), said means enabling the application module and the electrical applications controller to be disengaged and break electrical communication between them (column 10, lines 29-30), rotated 180 degrees and reengaged to reestablish electrical communication between them (Fig. 5).

Krech, Jr. et al. and McNutt et al. are analogous art because they are from the same field of endeavor, namely the transfer of data between memories.

At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the portability of the device of McNutt et al. to the architecture of

Krech et al. McNutt et al. teach the motivation for doing so is "a memory cartridge which may be reprogrammed in place by user command, then used to transport the user program and data to another PLC [programmable logic controller]" (column 4, lines 61-63). Therefore, it would have been obvious to combine Krech, Jr. et al. with McNutt et al. for the benefit of a portable data-transfer and storage device as specified in claim 7.

18. **Claim 12** is rejected under 35 U.S.C. 103(a) as being unpatentable over DeKoning et al. (US 6,178,520) in view of Baentsch et al. (US 6,272,607).

19. **With respect to claim 12**, DeKoning et al. disclose a method of installing a new memory that has a predetermined capacity and a new memory ID into a system that comprises a processor (112 of Fig. 1) and first and second old memories (110 of Fig. 1) having respective first and second memory IDs (column 4, lines 23-27), said memories capable of storing application data, comprising:

- removing the first of old memory from the system (column 4, lines 6-10);
- installing the new memory into the system (column 4, lines 10-12);
- determining whether the new memory ID matches either of the first or second memory IDs (column 4, lines 23-27); and
- replicating the application data from the second old memory to the new memory if the new memory ID does not match either of the first or second memory IDs, to maintain a redundant array of independent memories (column 1, lines 43-45 describe how "the remaining available data and/or redundancy data is used to recreate the data missing due to the failure of a single disk drive").

DeKoning does not teach the limitation wherein

- said new memory transmits an empty data indication to said processor if said new memory does not store any data, and said transmission enables said data replication.

However, Baentsch et al. disclose the limitation wherein

- said new memory transmitting an empty data indication to said processor if said new memory does not store any data (column 2, lines 64-65) and said transmission enables said data replication (column 3, lines 11-15).

DeKoning et al. and Baentsch et al. are analogous art because they are from the same field of endeavor, namely the transfer of data between memories.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to apply the empty data indication of Krech, Jr. et al. to the drive detector system of DeKoning et al. The motivation for doing so would have been to avoid overwriting critical data, because "the payload area [of an already allocated block] contains application data that is critical to the application" (column 2, lines 58-59). Therefore, it would have been obvious to combine DeKoning et al. with Baentsch et al. for the benefit of a hot-swap detection system that automatically detected a new disk drive, verified that it had no application data already on it and replicated data onto it to obtain the invention as specified in claim 12.

Response to Arguments

20. **With respect to applicant's amendment to claim 1** (page 10 of applicant's amendment) such that the memories are "removed from said processor" (lines 5 and 8), this is ambiguous as it could mean either that the memories are not connected to the

processor or are external to the processor. The examiner has given the claim its broadest reasonable interpretation and issued a new rejection under *35 USC § 102* according to the interpretation whereby "removed from said processor" means that the memory is external to the processor (see above paragraph 6).

21. **With respect to applicant's argument regarding the rejection of claim 2** (page 10 of applicant's amendment), the rejection was made using Krech, Jr. et al. (US 5,665,114), not "the Kamei patent". No reference authored by Kamei was used in the rejection. Regarding the substance of this argument under the assumption that the applicant was referring the Krech, Jr. et al. patent used in the rejection, RAM buffer (105 of Fig.1) is not a hub. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made under *35 USC § 103* (see above paragraph 15).

22. **With respect to applicant's argument regarding the rejection of claims 3-5** (page 11 of applicant's amendment), the rejection was made using Krech, Jr. et al. (US 5,665,114), not "the Kamei patent", as is asserted at the beginning of the argument. No reference authored by Kamei was used in the rejection. Regarding the substance of this argument under the assumption that the applicant was referring the Krech, Jr. et al. patent used in the rejection, the examiner has given the claim its broadest reasonable interpretation and concluded that the controller module of the claim could be a controller assembled permanently from smaller components; the graphics processor of Krech, Jr. et al. could also be considered modular, as it is assembled from smaller components. Therefore, this rejection stands as issued.

23. **With respect to applicant's argument regarding the rejection of claims 8 and 9** (page 12 of applicant's amendment), the examiner notes that although the memories are described as "detachable and replaceable" (paragraph 3, line 7) in applicant's argument, this language is not found in the claim. Given its broadest reasonable interpretation, the claim language is taught by Baentsch et al., as conceivably one memory was attached and held data before the other. Therefore, this rejection stands as issued.

24. **With respect to applicant's argument regarding the rejection of claim 12** (page 13-14 of applicant's amendment), the rejection has been withdrawn in light of the amendment to the claim. However, upon further consideration, a new ground of rejection is made under *35 USC § 103* (see above paragraph 19).

25. **With respect to applicant's argument regarding the rejection of claims 6 and 7** (page 13 of applicant's amendment), the examiner notes that the rejections to claims 3 and 4, upon which claims 6 and 7 depend, have been upheld, and therefore the rejections to claims 6 and 7 are upheld as well.

Conclusion

26. Claims 1-9 and 12 are subject to a second action non-final rejection.

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Hashimoto (US 5,117,395) teaches a system with removable FIFO memories.
- Shibata et al. (US 5,123,099) teach a redundant memory system with removable memories.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Golden whose telephone number is 571-272-5628. The examiner can normally be reached on Monday-Friday, 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James R. Golden
Patent Examiner
Art Unit 2187

January 19, 2006

B.R. Peeso
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2/3/06